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Design and Analysis of Hybrid 1-Bit Full Adder Circuit and Its Impact on 2-Bit Comparator: A Review

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Abstract: In this paper, a hybrid 1-bit full adder design employing both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported and it is incorporated in a 2-bit comparator design. The circuit was implemented using Tanner tools. Performance parameters such as power, delay, and layout area were compared with the existing designs such as classical CMOS full adder(C-CMOS),complementary pass-transistor logic(CPL), transmission gate adder(TGA) and so on. In comparison with the existing full adder designs, the present implementation was found to offer significant improvement in terms of power and speed and thus in a 2-bit comparator design.

Keywords: Carry propagation adder, hybrid design, low power, CMOS (Complementary Metal Oxide Semiconductor), high speed, Tanner tool.

I. INTRODUCTION

Increased usage of the battery-operated portable devices like cellular phones, personal digital assistants (PDAs) and notebooks demand VLSI and ultra large-scale integration designs with an improved power delay characteristics. Full adders, being one of the most fundamental building blocks of all the aforementioned circuit applications, remain a key focus domain of the researchers over the years. Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells. Adder core is the most critical building block in microprocessors and digital signal processors. In general, a one-bit full adder core has three inputs (A, B, and carry in Ci) and two outputs (sum S and carry out Co). The complex arithmetic circuits such as subtraction, multiplication, and division functions usually can be realized by co-operations of multiple adders. An adder performance affects the arithmetic system as a whole.

The designs, reported so far, may be broadly classified into two categories:
1) static style and
2) dynamic style.

Static full adders are generally more reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart.

Different logic styles tend to favor one performance aspect at the expense of others. Standard static CMOS, dynamic CMOS logic, complementary pass-transistor logic (CPL), and transmission gate full adder (TGA) are the most important logic design styles in the conventional domain. The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation. These designs exploit the features of different logic styles to improve the overall performance of the full adder.

The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count (as that of) but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing 32 transistors. However, CPL is not an appropriate choice for low-power applications. Because of its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs is the bottleneck of this approach.

The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance. Although the hybrid logic styles offers promising

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performance, most of these hybrid logic adders suffered from poor driving capability issue and their performance degrades drastically in the cascaded mode of operation if the suitably designed buffers are not included.

The main objective of this paper is to improve the different performance parameters like power, delay, and transistor count of the full adder compared with the already existing ones and incorporating them into a 2-bit comparator. The circuit was implemented using Tanner tools. The average power consumption of the proposed circuit was reduced dramatically by deliberate incorporation of very weak CMOS Inverters coupled with strong transmission gates.

II. FULL ADDER ARCHITECTURE

The proposed full adder circuit is represented by three blocks as shown in Fig. 1(a). Module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (Cout). Each module is designed individually such that the entire adder circuit is optimized in terms of power, delay, and area. These modules are discussed below in detail.

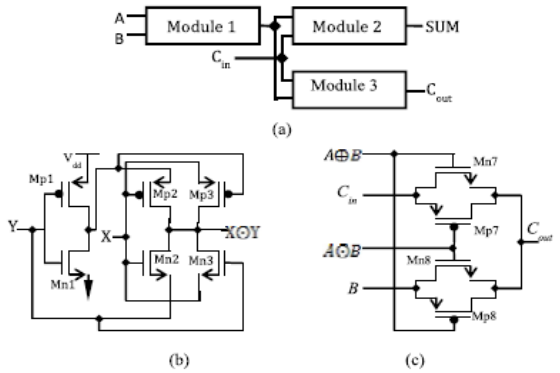

Fig. 1. (a) Schematic structure of proposed full adder. (b) XNOR module. (c) Carry generation module.

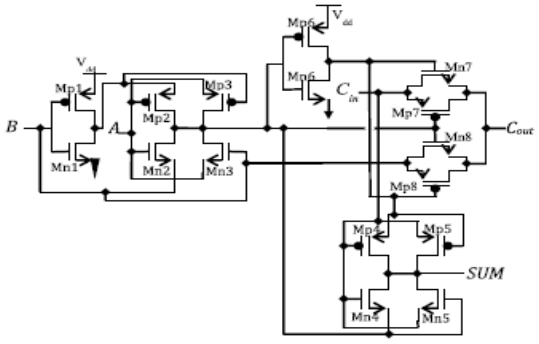

Fig 2. Detail circuit diagram of proposed full adder

A. Modified XNOR Module

In the proposed full adder circuit, XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore, this module is designed to minimize the power to the best possible extend with avoiding the voltage degradation possibility. Fig. 1(b) shows the modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter (channel width of transistors being small) formed by transistors Mp1 and Mn1 [Fig. 1(b)]. Full swing of the levels of output signals is guaranteed by level restoring transistors Mp3 and Mn3 [Fig. 1(b)]. In this paper, the XNOR module employed 6 T, having different transistor arrangement. The modified XNOR presented in this paper offers low-power and high-speed.

B. Carry Generation Module

In the proposed circuit, the output carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8 as shown in Fig. 1(c). The input carry signal (Cin) propagates only through a single transmission gate (Mn7 and Mp7), reducing the overall carry propagation path significantly. The deliberate use of strong transmission gates (channel width of transistors Mn7, Mp7, Mn8, and Mp8 is made large) guaranteed further reduction in propagation delay of the carry signal.

III. LITERATURE SURVEY

Literature survey is an important part of the project. It enables assimilation of knowledge required for the project right from the problem definition, finding a solution for the same and its execution. The following section summarizes the literature survey carried out for the project.

Kiran R. Barapatre, Mayur B. Petkar, Asmita R. Padole explains the concept of **"CMOS Full Adder for Energy Efficient Arithmetic Applications"[1].** In this, they say that Energy-Efficiency is one of the most required features in digital electronic systems for high-performance and/or portable applications which signify PDP, it measures the energy consumed per switching event. Also, they proved complementary CMOS is the logic style of choice for the implementation of combinational circuits, if low voltage, low power, and small power-delay products are of concern with relatively low area.

Mohammad Javad Zavarei, Ehsan Kargaran designed 1-bit full adder using hybrid-CMOS logic style presented a paper entitled as **"Design of new full adder cell using hybrid-CMOS logic style"[2]**. The new full adder is based on a novel XOR-XNOR circuit that outperforms its best counterpart showing 28% improvement in power-delay product (PDP). Design of proposed full adder is based on improvement in the PDP and it provides full-swing output with good driving capability. Simulations demonstrate that full adder successfully operates in the PDP compared to similar circuits.

"Design Analysis of XOR (4T) based Low Voltage CMOS Full Adder Circuit"[3], is a paper presented by **Subodh Wairya, Garima Singh,Vishant, R. K.Nagaria, S. Tiwari**. In this performance analysis of 1-bit full adder cell has been presented. Different adder logic styles have been implemented, simulated, analyzed and compared. Using the adder categorization and hybrid-CMOS design style, many full adders can be conceived. As an example, newly full adder has been designed using hybrid-CMOS

design style with pass transistor are presented that targets low PDP. The XOR based hybrid-CMOS full adder shows better performance than most of the other standard full-adder cells owing to the new design modules analysis is discussed.

"Architecture Of Adders Based On Speed , area And Power dissipation"[4], is a paper presented by **Prashanth.P and Prabhu Swamy**. In this a stacking pMOS transistor is introduced in 10-T and 11-T adder cells to reduce the leakage current of the circuit. Due to reduction of leakage current the power consumption is reduced. These adder circuits can be used for low power applications.

The paper entitled as **"Hybrid adders for high-speed arithmetic circuits: a comparison"[5],** presented by **Monico Linares Aranda, Ramon Báez, Oscar Gonzalez Diaz**. In this paper the most interesting topologies of one-bit hybrid full adders, are analyzed and compared for speed, power consumption, and power-delay product. Performance has been also compared for different supply voltage values. The simulation results show that the Chang adder is the best in terms of PDP figure of merit, however the Aguirre adder is the best in terms of driving capability even at low power supply.

The paper entitled **"A novel low-power full-adder cell for low voltage"[6],** presented by **Keivan Navi , Mehrdad Maeen, Vahid Foroutan, Somayeh Timarchi, Omid Kavehei**. They presents a novel low-power majority function-based 1-bit full adder that uses MOS capacitors (MOSCAP) in its structure. It can work reliably at low supply voltage. In this design, the time-consuming XOR gates are eliminated. The circuits being studied are optimized for energy efficiency at 0.18-µm CMOS process technology. The adder cell is compared with seven widely used adders based on power consumption, speed, power-delay product (PDP) and area efficiency.

Keivan Navi, Mohammad Hossein Moaiyeri, Reza Faghih Mirzaee, Omid Hashemipour, Babak Mazloom Nezhad proposed a concept of **"Two new low-power Full Adders based on majority-not gates"[7].** Two novel low-power 1-bit Full Adder cells have been proposed. Both circuits use only two majority-not gates, which are implemented using new methods. The first design used only capacitors and CMOS inverter gates, while the second one has benefited from a high-performance CMOS bridge circuit, which has improved the parameters of the first design. Low power consumption has been targeted at the circuit design level for both cells.

Chiou-Kou Tung, **Yu-Cherng Hung** gives the idea about new three-input exclusive OR (3-XOR) design, the new hybrid full adder is composed of pass-transistor logic and static CMOS logic**.** The main design objectives for the full adder core are providing not only low power and high speed but also with driving capability. The circuit is proven to have the minimum power consumption and the fastest response of carry out signal among the adders selected for comparison. Due to the low-power and high-speed properties, both the new exclusive OR circuit and the new full adder can be efficiently integrated in a system-on-a-chip (SoC) or an embedded system[8].

Sumeer Goel, **Ashok Kumar and Magdy A. Bayoumi** presented a paper entitled **"Robust, Energy-Efficient Full Adders for Deep-Submicrometer Design Using Hybrid-CMOS Logic Style"[9]**. The proposed hybrid-CMOS full adder has better performance than most of the standard full-adder cells. It performs well with supply voltage scaling and under different load conditions. When embedded in a four-operand CSA, it outperforms all the other adders making it suitable for larger adders. The proposed adder has better noise immunity as compared to the standard adder such as static CMOS, making it suitable for deep-submicrometer operation. We recommend the use of hybrid-CMOS design style for the design of high-performance circuits.

"A Review of 0.18-um Full Adder Performances for Tree Structured Arithmetic Circuits"[10], is a paper presented by **Chip-Hong Chang, Jiangmin Gu and Mingyan Zhang,** says that for full adder cell design, pass-logic circuit is thought to be dissipating minimal power and have smaller area because it uses less number of transistors. A hybrid full adder cell consisting of the XOR/XNOR, sum and carry out sub circuits, is proposed. The pass logic design style is used to efficiently generate the XOR and XNOR functions simultaneously and a good drivability carry out is generated by a complementary CMOS style circuit with regular layout.

Mingvan Zhang, Jiangmin Gu and Chip-Hong Chang presented a paper titled as **"A novel hybrid pass logic with static CMOS output drive full-adder cell",[11].** In this, investigation resulted in A novel design of a 1-bit full adder cell featuring hybrid CMOS logic style where the pass logic style has been used to efficiently generate the XOR and XNOR functions simultaneously and a good drivability carry out has been generated by a novel complementary CMOS style with regular structure. The circuit has shown to be power-delay efficient over a wide supply voltage ranges above 2.4V and is therefore suitable for constructing low power, high performance arithmetic logic unit for embedded applications

"Novel Design Methodology for High-Performance XOR-XNOR Circuit Design"[12], is a paper proposed by **Sumeer Goel, Mohamed A. Elgamel and Magdy A. Bayoumi**. Here they proposed and tested a novel design methodology for noise-immune low voltage XOR-XNOR circuits. The performance of the proposed circuits has been shown to outperform the compared ones, which can operate at low-voltages, and have good output levels. The proposed circuits haves been tested to be much noise-immune, energy-efficient and faster than the compared ones.

A. M. Shams, T. K. Darwish, M. A. Bayoumi presented a paper entitled "**Performance analysis of low-power 1-bit CMOS full adder cells"[13].** Here adder cell is anatomized into smaller modules. The modules are studied

and evaluated extensively. Several designs of each of them are developed, prototyped, simulated and analyzed. Twenty different 1-bit full-adder cells are constructed (most of them are novel circuits) by connecting combinations of different designs of these modules. Each of these cells exhibits different power consumption, speed, area, and driving capability figures. Two realistic circuit structures that include adder cells are used for simulation.

IV. APPLICATIONS

1) **Hassoune, D.Flandre, I.O'Connor & J. Legat** proposed a new structure of a hybrid full adder, namely, the branch based logic and pass-transistor (BBL-PT) cell, which is implemented by combining branch-based logic and pass-transistor logic. This leads to tremendous benefit for multiplier application. Also, the implementation of an 8-bit ripple carry adder based on the ULPFA is described. and comparisons between adders based on full adders from the prior art and ULPFA version demonstrate that development outperforms the static CMOS and the CPL full adders, particularly in terms of power consumption and PDP by at least a factor of two[14].

2) **D.Radhakrishnan** designed new adder cell that does not suffer from the threshold voltage drop in MOS transistors, but at the same time uses fewer transistors. This new cell can easily be adopted for low voltage operation as long as the supply voltage is not allowed to fall below 2|Vip|. This cell can then function as a library cell for the future design of low-power CMOS combinational circuits[15].

3) **M. Alioto, G. Di Cataldo, G. Palumbo** presented a paper which deals with the implementation of Full Adder chains by mixing different CMOS Full Adder topologies. The approach is based on cascading fast Transmission-Gate Full Adders interrupted by static gates having driving capability, such as inverters, thus exploiting the intrinsic low power consumption of such topologies. The obtained mixed-topology circuits are optimized in terms of delay by resorting to simple analytical models[16].

V.CONCLUSION

In this paper, a low-power hybrid 1-bit full adder has been proposed. The simulation was carried out using Tanner tool in 45-nm technology and compared with other standard design approaches like CMOS, CPL, TFA, TGA. The simulation results established that the proposed adder offered improved PDP compared with the earlier reports. The efficient coupling of strong transmission gates driven by weak CMOS inverters lead to fast switching speeds, lesser layout area. The proposed full adder is used in comparator design and results are compared with standard design approaches.

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